is driven from the first logic element onto the interconnect line using the first tristate driver;

dynamically tristating the first tristate driver; and

dynamically enabling a second tristate driver having an input coupled to a second logic element and an output directly connected to the interconnect line, such that a second signal is driven from the second logic element onto the interconnect line using the second tristate driver.

48. (Amended) A programmable logic integrated circuit comprising:

a programmable interconnect bus;

a plurality of logic elements configurable to perform logical functions;

a plurality of tristate devices coupled between the plurality of logic elements and the programmable interconnect bus;

a plurality of programmable memory cells coupled to the plurality of tristate devices to programmably enable and programmably tristate the plurality of tristate devices; and

tristate control logic having outputs coupled only to the plurality of tristate devices to dynamically enable and dynamically tristate the plurality of tristate devices.

52. (Amended) A programmable logic integrated circuit comprising:

a first logic element having a first output;

a first tristate driver having a first enable input, a second enable input, a second output, and a first input coupled to the first output;

a first programmable memory cell coupled to the first enable input;

a second logic element coupled to the second enable input;

a third logic element having a third output;

a second tristate driver having a third enable input, a fourth output, and a second input coupled to the third output;

a second programmable memory cell coupled to the third enable input; and

an interconnect line coupled to the second output and the fourth output, wherein the interconnect line is not coupled to the second input and the fourth input by a programmable connection, and the second logic element may dynamically tristate and dynamically enable the tristate driver.

55. (New) The method of claim 33 wherein the first tristate driver is dynamically tristated without writing to a memory cell.

56. (New) An integrated circuit comprising:
a first logic element having an output;
a first tristate driver having an input coupled to the output of the first logic element, and an output;
a second logic element having an output;
a second tristate driver having an input coupled to the output of the second logic element, and an output; and
an interconnect line coupled to the output of the first tristate driver and coupled to the output of the second tristate driver,
wherein the output of the first tristate driver is not coupled by a programmable connection to the interconnect line, the output of the second tristate driver is not coupled by a programmable connection to the interconnect line, and the first tristate driver and the second tristate driver may be dynamically tristated and enabled.

57. (New) The integrated circuit of claim 56 wherein the first tristate driver is dynamically tristated without writing to a memory cell.

58. (New) An integrated circuit comprising:
a first tristate driver coupled between a first logic element and a first interconnect line;

a second tristate driver coupled between a second logic element and a second interconnect line; and

a tristate control block having outputs coupled only to enable inputs of a plurality of tristate drivers,

wherein the plurality of tristate drivers comprises the first tristate driver and the second tristate driver.

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59. (New) The integrated circuit of claim 58 further comprising a third logic element coupled to the tristate control block.

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60. (New) The integrated circuit of claim 59 wherein the first tristate driver and the second tristate driver may be dynamically tristated and enabled.

61. (New) The integrated circuit of claim 60 wherein the first tristate driver and the second tristate driver are dynamically tristated without writing to a memory cell.